WHAT IS CLAIMED IS:

1. A duty cycle correction circuit for changing the duty cycle for a differential periodic signal, the duty cycle correction circuit including:

input circuitry for receiving a first differential signal, the differential signal including a first signal component and a complement signal component, each of the signal components having initial high and low signal levels and respective first and second DC bias levels, the input circuitry including a differential output having a first path for propagating the first signal component and a second path for propagating the complement signal component;

programmable load circuitry coupled to the differential output and having a programmable input, the load circuitry operative to programmably vary the DC bias level of at least one of the signal components; and

a differential gain amplifier coupled to the first differential output and disposed downstream of the load circuitry.

2. A duty cycle correction circuit according to claim 1 wherein the input circuitry comprises:

a differential buffer amplifier.

3. A duty cycle correction circuit according to claim 2 wherein the differential buffer amplifier comprises a CMOS differential buffer amplifier.

4. A duty cycle correction circuit according to claim 1 wherein the programmable load circuitry comprises:

first and second current sources coupled to the first and second paths.

5. A duty cycle correction circuit for changing the duty cycle for a differential periodic signal, the duty cycle correction circuit including:

means for receiving a first differential signal, the differential signal including a first signal component and a complement signal component, each of the signal components having initial high and low signal levels and respective first and second DC bias levels, the means for receiving including a differential output having a first path for propagating the first signal component and a second path for propagating the complement signal component;

means for programmably varying the DC bias level of at least one of the signal components; and

means for amplifying the first differential output and disposed downstream of the load circuitry.

6. A duty cycle correction circuit according to claim 5 wherein the means for receiving comprises input circuitry including a differential buffer amplifier.

7. A duty cycle correction circuit according to claim 5 wherein the means for programmably varying the DC bias level comprises:

means for loading the differential output and having a programmable input.

8. A duty cycle correction circuit according to claim 7 wherein the means for loading comprises programmable load circuitry including first and second current sources coupled to the first and second paths.

9. A duty cycle correction circuit according to claim 5 wherein the means for amplifying comprises a differential gain amplifier.

10. Automatic test equipment for testing semiconductor devices, the automatic test equipment including timing circuitry having:

a differential clock source for generating a differential clock signal;

fanout circuitry for distributing the differential clock source to a plurality of timing circuits;

a timing generator having an input for receiving a differential clock signal of a desired duty cycle; and

a duty cycle control circuit disposed at the input of the timing generator to selectively modify the duty cycle of the differential clock signal to match the desired duty cycle, the duty cycle control circuit including

input circuitry for receiving a first differential signal, the differential signal including a first signal component and a complement signal component, each of the signal components having initial high and low signal levels and respective first and second DC bias levels, the input circuitry including a differential output having a first path for propagating the first signal component and a second path for propagating the complement signal component;

programmable load circuitry coupled to the differential output and having a programmable input, the load circuitry operative to programmably vary the DC bias level of at least one of the signal components; and

a differential gain amplifier coupled to the first differential output and disposed downstream of the load circuitry.

11. A method of changing the duty cycle of a differential signal, the differential signal having a first signal component and a complement signal component, each of the signal components having initial high and low signal levels and respective DC bias levels, the method including the steps:

modifying the DC bias level of one of the signal components to a desired level, the modified signal component cooperating with the other signal component to form a modified differential signal; and

restoring the initial high and low signal levels.

12. A method according to claim 11 wherein the modifying step includes changing the DC bias level of one of the signal components until the average value of one component substantially equals the average value of the other component.

13. A method according to claim 11 wherein the modifying step includes:

buffering the differential signal with a differential buffer having a differential output; and

loading the differential output to form the modified differential signal.

14. A method according to claim 11 wherein the restoring step includes:

differentially amplifying the modified differential signal.